BE Semester- IVth (Biomedical Department) Question Bank

(DIGITAL DESIGN TECHNIQUES)

All questions carry equal marks (10 marks)

Q.1	Perform the following operation. (24.6)10 = ( )2 (615)8 = ( )16 (725.63)8 = ( )2 (35.48)10 = ( )Exceess-3
Q.2	Find 10's, 2's, 9's, 1's Complement following value: (3460)10 (7520)10 (101110)2 (1110110)2
Q.3	Convert Decimal to Binary: (513)10 (676)10 (105.3174)10 (119)10
Q.4	Convert Binary to Decimal: (1110100)2 (1010111)2 (110110)2 (1101.0101)2
Q.5	Convert decimal to hexadecimal: (227)10 (876)10 (93.76)10 (143)10
Q.6	Convert decimal to octal: (513)10 (676)10 (117)10 (126.43)10
Q.7	Solve the following: $(110101)_2 * (1001)_2$ $(100111)_2 - (100101)_2$ $(11100101)_2 - (1100111)_2$ $(1010)_2 * (11)_2$
Q.9	Solve using 10's complement method: 46370 – 09230 3240 – 6730

<table>
<tr><td>Q.10</td><td>Draw & Explain Half Adder & Full Adder.

F(x, y, z) = m (2, 4, 6, 7). Find its complement of F [F'(x, y, z)] & Derive max term.</td></tr>
<tr><td>Q.11</td><td>Perform binary addition of: 24 & 15, 85 & 22.</td></tr>
<tr><td>Q.12</td><td>Using 9's & 10's complement: (350) + (-500) & (250) + (-790)</td></tr>
<tr><td>Q.13</td><td>Define the following: Binary System, combinational logic, computer, digital logic, integrated circuit.</td></tr>
<tr><td>Q.14</td><td>Solve using 2's complement:

$(11011)_2 - (111)_2$

$(11010)_2 - (11110)_2$</td></tr>
<tr><td>Q.15</td><td>Following Truth Table:
a) Express F1 & F2 in products of maxterms.
b) Obtain the simplified function in sums of products.
c) Obtain the simplified function in Products of Sums.

<table>
<tr><th>X</th><th>Y</th><th>Z</th><th>F1</th><th>F2</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
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<tr><td>Q.16</td><td>Prove that NOR Gate is a Universal gate by drawing AND, OR, NOT, EX-OR using NOR</td></tr>
<tr><td>Q.17</td><td>Prove that NAND Gate is a Universal gate by drawing AND, OR, NOT, EX-OR using NAND.</td></tr>
<tr><td>Q.18</td><td>Perform F (x, y, z) = ∑m (0, 7, 8, 9, 10, 12) +∑d (2, 5, 13</td></tr>
<tr><td>Q.19</td><td>Solve using Mccluskey Method.
F(w, x, y, z) = ∑ (0, 2, 3, 6, 7, 8, 10, 12, 13)</td></tr>
<tr><td>Q.20</td><td>Solve using K-MAP Method:
A) Y = $\overline{A}\overline{B}C\overline{D}$ +ABC$\overline{D}$ +A$\overline{B}$C$\overline{D}$+ A$\overline{B}$CD + A$\overline{B}\overline{C}\overline{D}$ + AB$\overline{C}\overline{D}$ + $\overline{A}\overline{B}$CD+ $\overline{A}\overline{B}\overline{C}\overline{D}$
B) F (w, x, y, z) = ∑ (1,3,4,6,8,10,12,14).</td></tr>
</table>

Q.21	Explain the following in detail:RS FLIP FLOP, JK FLIP FLOP
Q.22	Draw & explain logic gates along with input output signals.
Q.23	Discuss different logic families in detail.
Q.24	What do you mean by multiplexer, Demultiplexer, encoder & decoder? Differentiate between them.
Q.25	Explain 4-bit synchronous & asynchronous up & down counter.
Q.26	What is counter? Explain in detail ripple counter
Q.27	Explain in detail 4 bit right & left shift register.
Q.28	Write a short note on RAM & ROM.
Q.29	Elaborate On I^2L, ECL, MOS, CMOS.
Q.30	Explain HDL based Digital design.
Q.31	Draw & explain even & odd parity generator using EX-OR gates.
Q.32	Explain the following in detail:T FLIP FLOP, D FLIP FLOP
Q.33	Explain in detail combinational PLDs.
Q.34	Draw & explain latch using NAND gates.
Q.35	Draw & explain latch using NOR gates
Q.36	Explain Codes for Detecting and Correcting Errors.
Q.37	What do you mean by three state devices? Explain comparator in detail.
Q.38	What do you understand by ALU? Explain its design in detail.
Q.39	Implement the following using don't care condition. Assume that both the normal & complement inputs are available: (With no more than 2 nor gates) F = A'B'C'+AB'D+A'B'CD' d= ABC+AB'D'
Q.40	Convert the following into other canonical form: F(A,B,C,D)=Σ(0,2,6,11,12,13) F(A,B,C,D)=Π(0,1,2,3,4,6,12)